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WORKMAN NYDEGGER
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60 EAST SOUTH TEMPLE
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SALT LAKE CITY, UT 84111

EXAMINER	
CONTINO, PAUL F	
ART UNIT	PAPER NUMBER
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/769,202	DUBE, JEAN-FRANCOIS
	Examiner	**Art Unit**
	Paul Contino	2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 29 November 2006.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7,9-11 and 20-37 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 12-19 is/are allowed.

6)☒ Claim(s) 1-7,9-11 and 20-37 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed November 29, 2006, on pages 14-16 of the Applicant's Remarks, have been fully considered but they are not persuasive.

The Examiner respectfully disagrees with the Applicant's arguments on pages 14 and 15 regarding the Wall prior art reference as failing to teach or suggest diagnostic functions different from one another. The Examiner interprets that executing a unique set of instructions resulting in varying amounts of functionality and monitoring of different conditions for each processor, as is stated in column 12 in lines 39-41 and 44-45, and column 13 lines 22-23 and 28, does teach a plurality of differing diagnostic functions. The specifics of each diagnostic function are not disclosed in, for example, claim 1, sufficiently to overcome the prior art reference Wall. The term function as claimed allows for a very broad and general interpretation. Such disclosure of specific functions, however, are present in, for example, claim 5, and further discussed in the Applicant's Remarks on pages 15 and 16, relating to diagnostic functions comprising a jammer, bit error rate tester, generator, and analyzer.

2. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., diagnostic functions comprising a jammer, generator, bit error rate tester, etc.) are not recited in, for example, the argued and rejected claim 1. Although the claims are interpreted in light of the

specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "the one of the plurality of different network diagnostic functions" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3, 4, 10, 20-24, 26, 27, and 31-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Wall et al. (U.S. Patent No. 6,507,923).

As in claim 1, Wall et al. discloses a diagnostic module, the diagnostic module *(Fig. 5 #60; column 7 lines 56-57)* comprising:

a bus interface configured to exchange data with a computer system bus *(Fig. 5 #s 68,80; column 8 lines 24-32, where data/control bus 68 and backplane 80 are interpreted as a computer system bus and bus interface, respectively)*;

one or more programmable logic modules *(Fig. 5 #74)*, each programmable logic module configured to process first bit files that cause the programmable logic module and at least one communicatively coupled port to interoperate to implement a first one of a plurality of different network diagnostic functions *(Fig. 7; column 8 lines 5-7, column 9 lines 22-29, column 12 lines 36-48, and column 14 lines 51-61, where the FPGA 92 is a component of the programmable logic module 74, channel 62/82 is interpreted as a port, and the program of instructions is interpreted as bit files)*, each programmable logic module including a clock configured to coordinate the transfer of data between the programmable logic module and the at least one communicatively coupled port *(column 9 lines 12-14 and column 10 line 65 through column 11 line 7)* and wherein each programmable logic module is further configured to process second bit files that cause the programmable logic module and at least one communicatively coupled port to interoperate to implement a second one of the plurality of different network diagnostic functions, wherein the second one of the plurality of network diagnostic functions is different from the first one of the plurality of different network diagnostic functions *(column 12 lines 36-47, column 12*

line 66 through column 13 line 2, column 13 lines 17-34, and column 14 lines 51-55, where it is interpreted that there is a program/bit file for each trac processor 150/152 of the programmable logic module 92, where each trac processor 150/152 implements a different respective function);

one or more ports, each port communicatively coupled to one of the one or more programmable logic modules, each port being network connectable to a network *(Fig. 5 #s 10,62,74; column 8 lines 5-8)*; and

a control module *(Fig. 5 #78)* communicatively coupled to the bus interface and communicatively coupled to each of the one or more programmable logic modules, the control module configured to coordinate the transfer of data between the bus interface and the one or more programmable logic modules *(column 12 lines 37-41 and line 67 through column 13 line 2)*.

As in claim 3, Wall et al. discloses the one or more programmable logic modules comprise one or more FPGAs *(Figs. 5,7; column 9 lines 24-25)*.

As in claim 4, Wall et al. discloses the one or more FPGAs comprise circuitry that, in response to receiving appropriate instructions, can implement any of the plurality of different network diagnostic functions *(column 12 lines 36-48)*.

As in claim 10, Wall et al. discloses one or more memory modules, each memory module communicatively coupled to a corresponding programmable logic module, each memory module

configured to store data for a corresponding programmable logic module *(Fig. 7; column 12 line 66 through column 13 line 2 and column 14 lines 51-55).*

As in claim 20, Wall et al. discloses in a computer system *(Fig. 5 #60; column 7 lines 56-57)*, a method for configuring a network diagnostic module *(column 12 lines 36-48 and column 14 lines 51-55)*, the method comprising the acts of:

receiving an indication that the network diagnostic module is to be configured to perform a first selected network diagnostic function *(column 12 lines 36-48 and column 14 lines 51-55, where the downloading of instructions to the FPGA 92 is interpreted as an indication for configuration)*;

receiving a first bit file for implementing the first selected network diagnostic function at one or more ports *(Fig. 7; column 8 lines 5-7, column 9 lines 22-29, column 12 lines 36-48, and column 14 lines 51-61, where channel 62/82 is interpreted as a port and the program of instructions is interpreted as a bit file)*, the one or more ports interfacing with the network *(Fig. 5 #s 10,62,74; column 8 lines 5-8)*;

identifying a reconfigurable programmable logic module that controls the one or more ports *(Fig. 5; column 9 lines 24-28, where programmable logic FPGA 92/94 is interpreted as controlling ports 62; an FPGA is inherently reconfigurable)*; and

loading at least a portion of the received first bit file at the identified reconfigurable programmable logic module to cause the one or more ports to be configured to perform the first selected network diagnostic function *(column 12 lines 36-48 and column 14 lines 51-55)*;

receiving an indication that the network diagnostic module is to be configured to perform a second selected network diagnostic function *(column 12 lines 36-47, column 12 line 66 through column 13 line 2, column 13 lines 17-34, and column 14 lines 51-55, where it is interpreted that each trac processor 150/152 implements a different respective function)*;

receiving a second bit file for implementing the second selected network diagnostic function at one or more ports, the one or more ports interfacing with the network *(column 12 lines 36-47, column 12 line 66 through column 12 line 2, column 13 lines 17-34, and column 14 lines 51-55, where it is interpreted that there is a program/bit file for each trac processor 150/152 of the programmable logic module 92, where each trac processor 150/152 implements a different respective function)*; and

loading at least a portion of the received second bit file at the identified reconfigurable programmable logic module to cause the one or more ports to be configured to perform the second selected network diagnostic function, wherein the second selected network diagnostic function is different from the first selected network diagnostic function *(column 12 lines 36-47, column 12 line 66 through column 12 line 2, column 13 lines 17-34, and column 14 lines 51-55).*

As in claim 21, Wall et al. discloses the act of receiving an indication that the network diagnostic module is to be configured to perform the first or second selected network diagnostic function comprises an act of receiving user-input at an input device coupled to the computer system or a remote computer system *(Fig. 5 #90; column 9 lines 37-45 and column 10 lines 8-27).*

As in claim 22, Wall et al. discloses the act of receiving a bit file comprises an act of receiving a first or second bit file containing instructions that, when loaded at a programmable logic module, cause the programmable logic module and the one or more ports to interoperate to implement the first or second selected network diagnostic function *(column 9 lines 10-23, column 12 lines 36-48, and column 14 lines 51-55).*

As in claim 23, Wall et al. discloses the act of receiving a first or second bit file comprises an act of receiving a first or second bit file containing circuit design data that, when loaded at a programmable logic module, cause the programmable logic module and the one or more ports to interoperate to implement the first or second selected network diagnostic function *(column 9 lines 10-23, column 12 lines 36-48, and column 14 lines 51-55, where as aspect of programming an FPGA is that it uses instructions to [re]configure the hardware layout of the FPGA in order to alter the functionality – see included "How Programmable Logic Works" on pages 4-6 – in which the instructions and FPGA program are interpreted as circuit design data).*

As in claim 24, Wall et al. discloses the act of receiving a first or second bit file comprises an act of receiving a first or second bit file for implementing a port personality *(column 8 lines 5-10, column 12 lines 36-41, and column 14 lines 51-55).*

As in claim 26, Wall et al. discloses the act of loading at least a portion of the received second bit file at the identified programmable logic module comprises an act of reconfiguring the one or more ports from being configured to perform the first selected network diagnostics

function to being configured to perform the second selected network diagnostic function *(column 14 lines 47-63, where the FPGA 92 is loaded with a bit file [instructions] and configures the ports/channels 82/62 to perform either the diagnostic function of filtering or the diagnostic function of monitoring).*

As in claim 27, Wall et al. discloses the act of loading at least a portion the received first or second bit file at the identified programmable logic module comprises an act of loading a portion of the first or second bit file for implementing a network analyzer *(column 12 lines 36-48, where programmable logic module 74 housing FPGA 92 is interpreted as a network analyzer).*

As in claim 31, Wall et al. discloses the act of loading the at least a portion of the first or second bit file at the identified programmable logic module comprises an act of loading instructions that cause the one or more ports to be configured to perform the first or second selected network diagnostic function *(column 9 lines 10-23, column 12 lines 36-48, and column 14 lines 51-55).*

As in claim 32, Wall et al. discloses the act of loading the at least a portion of the first or second bit file at the identified programmable logic module comprises an act of loading circuit data that causes the one or more ports to be configured to perform the first or second selected network diagnostic function *(column 9 lines 10-23, column 12 lines 36-48, and column 14 lines 51-55, where as aspect of programming an FPGA is that it uses instructions to [re]configure the*

hardware layout of the FPGA in order to alter the functionality – see included "How Programmable Logic Works" on pages 4-6 – in which the instructions and FPGA program are interpreted as circuit design data).

As in claim 33, Wall et al. discloses an act of transferring network diagnostic data through the one or more ports in accordance with the first or second selected network diagnostic function *(column 9 line 10 through column 10 line 27).*

As in claim 34, Wall et al. discloses a computer program product *(Fig. 5 #60; column 7 lines 56-57)* comprising one or more computer-readable media having stored thereon computer executable instructions that, when executed by a processor, cause the computer system to perform the following:

receive an indication that a network diagnostic module is to be configured to perform first and second selected network diagnostic function *(column 12 lines 36-48 and column 14 lines 51-55, where the downloading of instructions to the FPGA 92 is interpreted as an indication for configuration; column 12 lines 36-47, column 12 line 66 through column 12 line 2, column 13 lines 17-34, and column 14 lines 51-55, where it is interpreted that there is a program/bit file for each trac processor 150/152 of the programmable logic module 92)*;

receive a first bit file for implementing the first selected network diagnostic function at one or more ports *(Fig. 7; column 8 lines 5-7, column 9 lines 22-29, column 12 lines 36-48, and column 14 lines 51-61, where channel 62/82 is interpreted as a port and the program of instructions is interpreted as a bit file)* and receive a second bit file for implementing the second

selected network diagnostic function at the one or more ports, the one or more ports interfacing with the network *(Fig. 5 #s 10,62,74; column 8 lines 5-8, column 12 lines 36-47, column 12 line 66 through column 13 line 2, column 13 lines 17-34, and column 14 lines 51-55, where it is interpreted that there is a program/bit file for each trac processor 150/152 of the programmable logic module 92, where each trac processor 150/152 implements a different respective function)*;

identify a reconfigurable programmable logic module that controls the one or more ports *(Fig. 5; column 9 lines 24-28, where programmable logic FPGA 92/94 is interpreted as controlling ports 62; and FPGA is inherently reconfigurable)*;

load the at least a portion of the first received bit file at the identified reconfigurable programmable logic module so as to cause the one or more ports to be configured to perform the first selected network diagnostic function *(column 12 lines 36-48 and column 14 lines 51-55)*; and

loading at least a portion of the second received bit file at the identified reconfigurable logic module to cause the one or more ports to be configured to perform the second selected network diagnostic function, wherein the second selected network diagnostic function is different from the first selected network diagnostic function *(column 12 lines 36-47, column 12 line 66 through column 12 line 2, column 13 lines 17-34, and column 14 lines 51-55, where it is interpreted that there is a program/bit file for each trac processor 150/152 of the programmable logic module 92)*.

As in claim 35, Wall et al. discloses the one or more computer-readable media comprise physical storage media *(column 10 lines 15-19)*.

As in claim 36, Wall et al. discloses the one or more computer-readable media comprise system memory *(column 10 lines 15-19)*.

As in claim 37, Wall et al. discloses a network diagnostic module *(Fig. 5 #60; column 7 lines 56-57)* configured to:

receive a first bit file, the first bit file including instructions or data for implementing a first selected network diagnostic function at one or more ports *(Fig. 7; column 9 lines 22-29, column 12 lines 36-48, and column 14 lines 51-61, where channel 62 is interpreted as a port and the program of instructions is interpreted as a bit file)*, the first selected network diagnostic function selected from among a plurality of different network diagnostic functions that can be implemented at the network diagnostic module *(column 10 lines 8-27)*, the one or more ports interfacing with a network *(Fig. 5 #s 10,62,74; column 8 lines 5-8)*;

identify a reconfigurable programmable logic module that controls the one or more ports *(column 8 lines 5-7, column 9 lines 10-23, column 12 lines 36-48, and column 14 lines 51-55, where an FPGA is inherently reconfigurable)*; and

load the included instructions or data at the identified reconfigurable programmable logic module to cause the reconfigurable programmable logic module and the one or more ports to interoperate to implement the first selected network diagnostic function *(column 9 lines 10-23, column 12 lines 36-48, and column 14 lines 51-55)*, wherein the reconfigurable programmable logic module and the one or more ports are configured to interoperate to implement a second selected network diagnostic function upon receipt and loading of instructions or data of a second

bit file, wherein the second selected network diagnostic function is different from the first selected network diagnostic function *(column 12 lines 36-47, column 12 line 66 through column 13 line 2, column 13 lines 17-34, and column 14 lines 51-55, where it is interpreted that there is a program/bit file for each trac processor 150/152 of the programmable logic module 92).*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wall et al. in view of Kowert (U.S. Patent No. 5,649,129).

As in claim 2, Wall et al. teaches of a network diagnostics module and a bus interface. However, Wall et al. fails to teach of a PCI bus interface. Kowert teaches of a PCI bus interface *(column 6 lines 5-6).*

It would have been obvious to a person skilled in the art at the time the invention was made to have included the PCI bus interface as taught by Kowert in the invention of Wall et al. This would have been obvious because the invention of Kowert offers a high performance, fault tolerant, and resource efficient means of analyzing a network *(column 3 lines 21-35).* Further,

the invention of Kowert connects a network analyzer card with a computer system bus via an industry standard PCI interface *(Kowert: Fig. 1; column 6 lines 5-9)*, similar to the analyzer card connection to the system bus via a backplane as taught by Wall et al. *(Wall et al.: Fig. 5 #s 74,80,68)*.

* * *

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wall et al. in view of Small Form Factor (Whatis.com definition – see included literature).

As in claim 6, Wall et al. teaches of a Fibre Channel network with interface ports *(Fig. 5 #62; column 7 line 57)*. However, Wall et al. fails to teach of a small form factor pluggable connector. Small Form Factor teaches of a small form factor connector for a fiber optic system *(paragraphs 1-5)*.

It would have been obvious for a person skilled in the art at the time the invention was made to have included the small form factor connector as taught by Small Form Factor in the invention of Wall et al. This would have been obvious because use of a small form factor pluggable connector offers a flexible, versatile, and cost efficient network connection solution *(paragraph 2)*.

* * *

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wall et al. in view of Small Form Factor (Whatis.com definition – see included literature), further in view of Gigabit Interface Converter (Whatis.com definition – see included literature).

As in claim 7, Wall et al. teaches of a Fibre Channel network with interface ports *(Fig. 5 #62; column 7 line 57)*. However, Wall et al. fails to teach of a small form factor pluggable connector. Small Form Factor teaches of a small form factor connector for a fiber optic system *(paragraphs 1-5)*. Gigabit Interface Converter teaches of a 10 Gigabit small form factor pluggable *(paragraph 1)*.

It would have been obvious for a person skilled in the art at the time the invention was made to have included the small form factor connector as taught by Small Form Factor in the invention of Wall et al. This would have been obvious because use of a small form factor pluggable connector offers a flexible, versatile, and cost efficient network connection solution *(paragraph 2)*.

It would have been obvious for a person skilled in the art at the time the invention was made to have included the 10 Gigabit small form factor pluggable as taught by Gigabit Interface Converter in the combined invention of Wall et al. and Small Form Factor. This would have been obvious because use of a 10 Gigabit small form factor pluggable is economical *(paragraph 2)*. Further, the combined invention of Wall et al. and Small Form Factor offers explicit teaching of a Gigabit pluggable *(Small Form Factor: paragraph 4)*.

* * *

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wall et al. in view of Official Notice.

As in claim 11, Wall et al. teaches the software configurable network diagnostic module comprises a plurality of circuitry and components *(Figs. 5,7; columns 7-12)*. However, Wall et al. fails to teach of a printed circuit board. The Examiner takes Official Notice that it was well-known to one of ordinary skill in the art at the time of the Applicant's invention to implement circuitry, such as processors, memory, network cards, etc. on a printed circuit board.

It would have been obvious to a person skilled in the art to have implemented the circuitry as taught by Wall et al. as components on a printed circuit board. This would have been obvious because a printed circuit board offers a cost-effective and spatially compact means of organizing circuitry in a computer system.

* * *

9. Claims 9 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wall et al. in view of Wang et al. (U.S. PGPub 2004/0254779).

As in claim 9, Wall et al. teaches of address information identifying a programmable logic module *(column 14 lines 19-39)*. However, Wall et al. fails to teach of the control module processing the address information. Wang et al. teaches of a control module processing address

information identifying a programmable logic module *(Figs. 3 and 4; paragraphs [0052] and [0057] where an FPGA 58 is interpreted as a resource that the controller 50 processed information containing its identification).*

It would have been obvious to a person skilled in the art at the time the invention was made to have included the control address processing as taught by Wang et al. in the invention of Wall et al. This would have been obvious because the invention of Wang et al. affords a highly scalable, flexible, and resource-efficient means for programming of a programmable device in a diagnostic system *(paragraphs [0022] and [0023]).*

As in claim 25, Wall et al. teaches of address information identifying a programmable logic module *(column 14 lines 19-39).* However, Wall et al. fails to teach of the address information being associated with the bit file [instructions]. Wang et al. teaches of utilizing processing address information with a bit file [instructions] to identify a programmable logic module *(Figs. 3 and 4; paragraphs [0052] and [0057] where an FPGA 58 is interpreted as a resource that the controller 50 processed information containing its identification).*

It would have been obvious to a person skilled in the art at the time the invention was made to have included the control address processing as taught by Wang et al. in the invention of Wall et al. This would have been obvious because the invention of Wang et al. affords a highly scalable, flexible, and resource-efficient means for programming of a programmable device in a diagnostic system *(paragraphs [0022] and [0023]).*

* * *

10. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wall et al. in view of Lesea (U.S. PGPub 2003/0023912).

As in claim 29, Wall et al. teaches of loading instructions into a programmable logic module. However, Wall et al. fails to teach of the instructions are for implementing a generator. Lesea teaches of a generator *(paragraph [0025])*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included instructions for implementing a generator as taught by Lesea in the invention of Wall et al. This would have been obvious because the invention of Lesea because use of an FPGA offers a fast and resource-efficient means for diagnostic network testing *(paragraph [0006] lines 6-8)*.

As in claim 30, Wall et al. teaches of loading instructions into a programmable logic module. However, Wall et al. fails to teach of the instructions are for implementing a bit error rate tester. Lesea teaches of a bit error rate tester *(paragraph [0025])*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included instructions for implementing a bit error rate tester as taught by Lesea in the invention of Wall et al. This would have been obvious because the invention of Lesea because use of an FPGA offers a fast and resource-efficient means for diagnostic network testing *(paragraph [0006] lines 6-8)*.

* * *

11. Claim 28 is rejected under 35 U.S.C. 103(a) as being obvious over Wall et al. in view of Oyadomari et al. (U.S. PGPub 2005/0060413).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As in claim 28, Wall et al. teaches of a programmable logic module. However, Wall et al. fails to teach implementing a jammer. Oyadomari et al. teaches operating a network analyzer as a jammer *(paragraph [0043])*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the jammer as taught by Oyadomari et al. in the invention of Wall et al. This would have been obvious because the invention of Oyadomari et al. offers multiple means of diagnosing a network in order to improve the fault tolerance of a system *(paragraphs [0042]-[0044])*.

Allowable Subject Matter

12. Claims 12-19 are allowed.

13. The following is a statement of reasons for the indication of allowable subject matter:

The claims are allowed based on the level of diagnostic configurability exhibited by each respective diagnostic module within the confines of the limitations of the invention as claimed.

14. Claim 5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PFC
1/8/2006

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